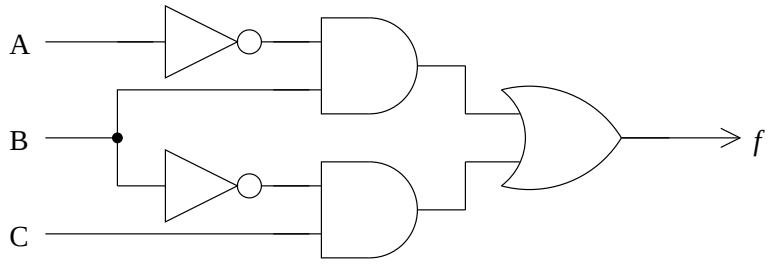
CSC 258 Lab 1

Part 1: Logic Gate Networks

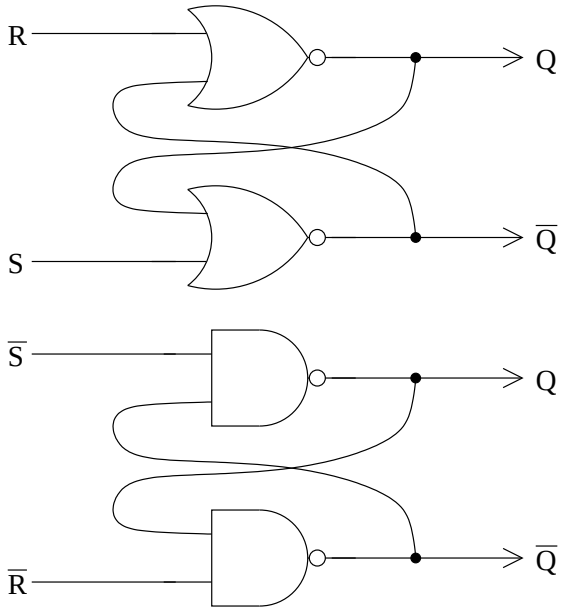
(a) Write out the truth-table of the following circuit. Build the circuit and verify its operation by running through all possible input combinations and comparing the output to the truth table.



(b) Design, build, and test an equivalent circuit using a minimal number of NAND gates (and no other kinds of gates). (That is, draw your gate diagram, build the circuit, and verify it against the truth table you wrote out for part (a).)

Part 2: Latches

(a) Investigate and explain the operation of each of the two SR latches shown below. Build and test each using two LEDs to show the state of the outputs Q and $\overline{Q}$.

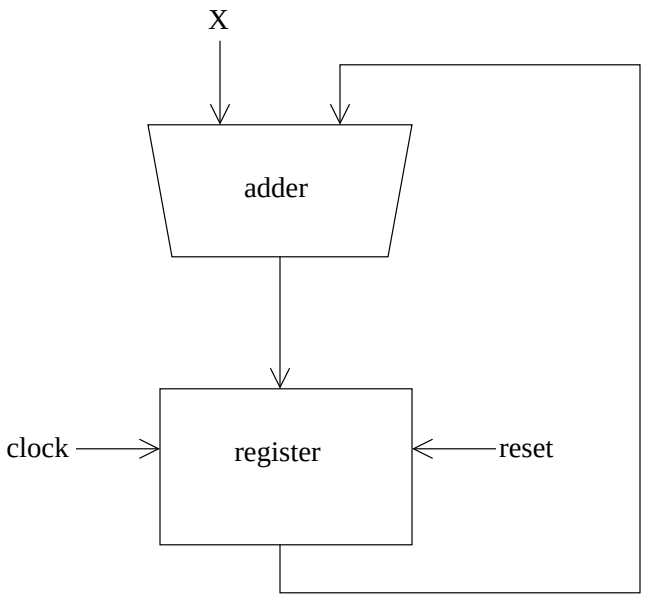


(b) [to think about] Under what circumstances would we prefer the second circuit to the first?

(over)

Part 3: Accumulator

Construct a four-bit version of the following circuit containing an adder (74LS283) and a master-slave-flip-flop register (74LS175). The four-bit output of the register should be connected to the output LEDs as well as back into the adder.



‘‘Clock’’ and ‘‘reset’’ each correspond to one input switch. ‘‘X’’ is four input switches, constituting a four-bit binary number.

The idea is that we add a list of numbers by presenting one value at a time. First, we use the RESET line to clear the register to the value zero. Then, we supply the first operand at ‘‘X’’ and raise the clock to 1, then back to 0. At this point, the contents of the register is equal to the first operand value. We can now supply another operand at ‘‘X’’, raise the clock briefly to 1, and the contents of the register will then be the sum.

An arbitrarily long list of numbers can be added this way (provided that the sum can fit in the supplied number of bits).

Does the register need to be composed of master-slave flip-flops for this design, or would clocked latches suffice? Explain.