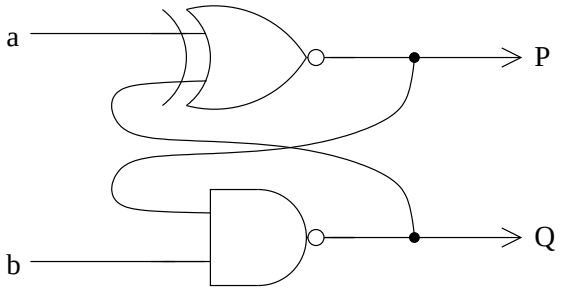
CSC 258 Assignment 2, Fall 2008

Due by 5:00 p.m., Friday October 17, 2008; no late assignments without written explanation.

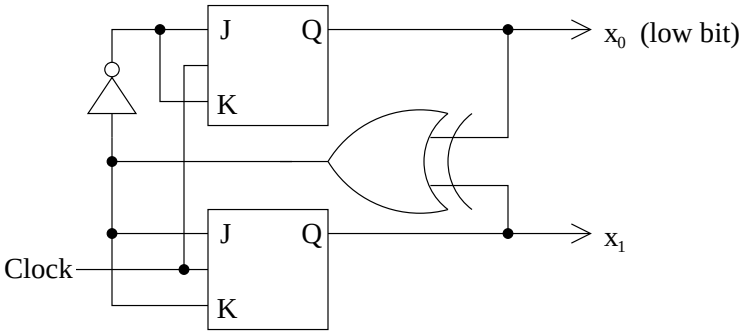
1. Here is a sequential circuit:



(a) List all of the possible stable states for each of the possible four input combinations, by stating the outputs of each gate (i.e. values P and Q).

(b) Can this circuit be used as a one-bit data latch? Explain how or explain why not.

2. The following circuit counts clock pulses, but its output is 0, 1, 3, 2, 0, 1, ... rather than the familiar 0, 1, 2, 3, 0, 1, ... :



Design a three-bit ‘‘counter’’ which counts 0, 3, 6, 4, 5, 6, 7, 0, 3, 6, 4, 5, 6, 7, ...
Be sure to label which are the three output lines clearly.
Show your work (at least, state your formulas for the various inputs).

(Note: You can use four flip-flops if you like, and any other standard combinational and sequential circuit components. However, a smaller circuit is better.)

(over)

3. Design a hardware stack to hold a maximum of four values, each consisting of one bit. The stack has the following input lines:

Clock
POP
PUSH
input data

and a single output line. The output line always reports the current top of the stack.

(Recall that a stack pushes data onto the top of the stack, and pops data from the top of the stack. In other words, last in, first out. If more than four values are pushed on, older values are discarded.)

You may use any standard combinational and sequential circuit components.

Remember:

This assignment is due at 5:00 p.m. on Friday October 17, 2008 (in the drop-box in BA 2220). Late assignments are not ordinarily accepted and *always* require a written explanation. If you are not finished your assignment by the submission deadline, you should just submit what you have, for partial marks.

Despite the above, I'd like to be clear that if there *is* a legitimate reason for lateness, please do submit your assignment late and send me that written explanation.